AMENDMENTS TO THE CLAIMS

Applicants submit below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Currently amended) A video decoding circuit comprising:

a first video data processor;

a second video data processor; and

a connection connecting said first video data processor and said second data processor;

wherein said first video data processor is arranged to receive a first signal comprising encoded video data, process said first signal to provide a second signal and output said second signal, said first video data processor being arranged to process said first signal dependent on at least part of said received first signal, and

said second video data processor comprising a predictor constructor, said second video data processor is arranged to receive at least a part of said second signal, process said at least a part of said second signal to provide a third signal, and output said third signal, said second and third signals comprising a decoded video image stream wherein a part of said second signal comprises a picture level parameter word which comprises coding standard information, said coding standard information ~~defining variations in the type of data~~ indicating which of a plurality of encoding methods was used to encode the encoded video data, and

said second video data processor is arranged to process said at least part of said second signal dependent on the format of the data received.

2. (Original) A circuit as claimed in claim 1, wherein said first video data processor is arranged to variable length decode said received first signal to produce a decoded first signal.

3. (Original) A circuit as claimed in claim 2, wherein said first video data processor is arranged to separate said first signal data into at least a first part and a second part,

wherein said first part comprises at least one of:

pixel data;

residual data, and

wherein said second part comprises motion vector data.

4. (Original) A circuit as claimed in claim 3, wherein said first video data processor is arranged to inverse quantize said first part of said first signal.

5. (Previously presented) A circuit as claimed in claim 3, wherein said first video data processor is arranged to spatial domain transform said first part of said first signal.

6. (Previously presented) A circuit as claimed in claim 4, wherein said first video data processor is arranged to combine said inverse quantized first part of said first signal with said second part of said first signal.

7. (Previously presented) A circuit as claimed in claim 1, wherein said second video data processor is arranged to interpolate at least a first part of said second signal.

8. (Original) A circuit as claimed in claim 7, wherein said second video data processor is arranged to interpolate at least a first part of said second signal using one of horizontal and vertical interpolation.

9. (Original) A circuit as claimed in claim 8, further comprising a memory, said second video data processor being arranged to store said interpolated part of said second signal in said memory.

10. (Previously presented) A circuit as claimed in claim 8, wherein said second video data processor is arranged to interpolate said stored interpolated first part of said second signal using the other one of horizontal and vertical interpolation.

11. (Previously presented) A circuit as claimed in claim 7, wherein said second video data processor is arranged to combine said interpolated part of said second signal and a further part of said second signal, wherein said interpolated part of said second signal comprises an estimated macro block, and said further part of said second signal comprises residual error data.

12. (Previously presented) A circuit as claimed in claim 12, wherein said second video data processor is arranged to filter at least one of said at least one part of said second signal and said third signal.

13. (Original) A circuit as claimed in claim 12 wherein said filter comprises at least one of a de-ringing filter and a deblocking filter.

14. (Currently amended) A circuit as claimed in claim 1, wherein said coding standard information defines variations in the type of data ~~said connection comprises a bus connecting said first and second video data processors~~.

15. (Currently amended) A circuit as claimed in claim 14, wherein said connection comprises a bus connecting said first and second video data processors, and wherein the circuit further comprising a memory device, said memory device being connected to said bus.

16. (Original) A circuit as claimed in claim 15, wherein said first video data processor has an output for outputting said second signal to said memory device via said bus.

17. (Original) A circuit as claimed in claim 16, wherein said second video data processor has an input for receiving said parts of said second signal from said memory device via said bus.

18. (Previously presented) A circuit as claimed in claim 1, wherein said connection comprises a data interconnect, said data

interconnect directly connecting said first video data processor and said second video data processor.

19. (Original) A circuit as claimed in claim 18, wherein said first video data processor has an output for outputting said second signal to said data interconnect.

20. (Previously presented) A circuit as claimed in claim 18, wherein said second video data processor has an input for receiving said parts of said second signal from said data interconnect.

21. (Previously presented) A circuit as claimed in claim 20, wherein said connection comprises a bus connecting said first and second video data processors and further comprising a memory device, said memory device being connected to said bus wherein said second video data processor receives part of said parts of said second signal from said data interconnect and part of said parts of said second signal from said bus.

22. (Currently amended) A circuit as claimed in claim 1, wherein the coding standard information indicates a format of the encoded video data corresponding to the encoding method used to encode the encoded video, and wherein said first signal is at least one of:

a MPEG2 encoded video stream;

a H. 263 encoded video stream;

a RealVideo9 encoded video stream;

a Windows media player encoded video stream;

a H. 264 encoded video stream.

23. (Previously presented) A circuit as claimed in claim 1, wherein said second signal comprises at least one of:

buffer base address word;

picture level parameter header word;

macro-block header word;

slice parameter word;

motion vector horizontal luma word ;

motion vector vertical luma word;

motion vector horizontal chroma word ;

motion vector vertical chroma word;

pixel data reference word and

pixel data residual word.

24. (Previously presented) A circuit as claimed in claim 1, wherein said first video data processor comprises a data packer.

25. (Previously presented) A circuit as claimed in claim 1, wherein said second video data processor comprises a data packer.

26. (Previously presented) A circuit as claimed in claim 24, wherein said data packer comprises: an input, said input being arranged to receive said second signal, said second signal comprising data words; means for ordering said data words; and an output, said output being arranged to transmit data packets comprising ordered data words.

27. (Previously presented) An integrated circuit comprising a circuit as claimed in claim 1.

28. (Previously presented) A circuit as claimed in claim 1, wherein said first video data processor comprises a very long instruction word processor.

29. (Original) A circuit as claimed in claim 28, wherein said very long instruction word processor is adapted to process said first signal further dependent on a set of instructions stored in a memory.

30. (Previously presented) A circuit as claimed in claim 1, wherein said second video data processor comprises a programmable processor.

31. (Currently amended) A video decoding method comprising the steps of:

receiving at a first video data processor a first signal comprising encoded video data,

processing said first signal to provide a second signal dependent on at least part of said first signal,

outputting said second signal,

receiving at least a part of said second signal at a second video data processor,

processing said at least part of said second signal within the second video processor predictor constructor to provide a third signal, and

outputting said third signal,

wherein said second and third signals comprise a decoded video image stream, wherein said step of outputting said second signal comprises the step of outputting a parameter word which comprises coding standard information, the coding standard information ~~defining variations in the type of data~~ indicating which of a plurality of encoding methods was used to encode the encoded video data, and said step of processing said at least part of said second signal is dependent on the format of the video data received.

32. (Original) A method as claimed in claim 31, wherein said step of processing said first signal comprises the step of variable length decoding said first signal.

33. (Previously presented) A method as claimed in claim 31, wherein said step of processing said first signal comprises the step of separating said first signal into at least a first part and a second part,

wherein said first part comprises at least one of:

pixel data;

residual data, and

wherein said second part comprises motion vector data.

34. (Original) A method as claimed in claim 33, wherein said step of processing said first signal further comprises the step of inverse quantizing said first part of said first signal.

35. (Previously presented) A method as claimed in claim 33, wherein said step of processing said first signal further comprises the step of spatial domain transforming said first part of said first signal.

36. (Previously presented) A method as claimed in claim 34, wherein said step of processing said first signal further comprises the step of combining said inverse quantized first part of said first signal with said second part of said first signal.

37. (Previously presented) A method as claimed in claim 31, wherein said step of processing at least a part of said second signal further comprises the step of interpolating at least a first part of said second signal.

38. (Original) A method as claimed in claim 37, wherein said step of interpolating at least a first part of said second signal comprises the step of interpolating at least a first part of said second signal using one of horizontal and vertical interpolation.

39. (Original) A method as claimed in claim 38, wherein said step of interpolating further comprises storing said interpolated part of said second signal.

40. (Previously presented) A method as claimed in claim 38, wherein said step of interpolating further comprises interpolating said interpolated part of said second signal using the other one of horizontal and vertical interpolation.

41. (Previously presented) A method as claimed in claim 37, wherein said step of processing at least part of said second signal further comprises combining said interpolated part of said second signal and a further part of said second signal, wherein said interpolated part of said second signal comprises an estimated macro block, and said further part of said second signal comprises residual error data.

42. (Currently amended) A method as claimed in claim 31, further comprising a further[[,]] step of further processing at least a part of said second signal wherein said further processing step comprises the step of filtering, wherein said step of filtering comprises at least one of the steps:

de-ringing filtering and de-blocking filtering.

43. (Previously presented) A method as claimed in claim 31, wherein said step of outputting said second signal further comprises the step of storing said second signal in a memory.

44. (Previously presented) A method as claimed in claim 40, wherein said step of receiving at least part of said second signal comprises receiving said at least part of said second signal directly from the first video data processor.

45. (Currently amended) A method as claimed in claim [[40]] 43, wherein said step of receiving at least part of said second signal comprises receiving a first part of said at least part of said second signal directly from said first video data processor and a second part of said at least part of said second signal from said memory.

46. (Previously presented) A method as claimed in claim 31, wherein said step of processing said first signal further comprises the step of packetizing said second signal.

47. (Previously presented) A method as claimed in claim 31, further comprising the steps of:

packetizing said at least part of said second signal;

storing said at least part of said second signal in a memory; and

receiving said at least part of said stored second signal from said memory.

48. (Canceled)

49. (Currently amended) A computer readable storage device comprising computer readable instructions, which, when executed by a processor, carry out a video decoding method comprising the steps of:

receiving at a first video data processor a first signal comprising encoded video data,

processing said first signal to provide a second signal dependent on at least part of said first signal, outputting said second signal, receiving at least a part of said second signal at a second video data processor, processing said at least part of said second signal within the second video processor predictor constructor to provide a third signal, and outputting said third signal, wherein said second and third signals comprise a decoded video image stream, characterised wherein said step of outputting said second signal comprises the step of outputting a parameter word which comprises coding standard information, the coding standard information ~~defining variations in the type of data~~ indicating which of a plurality of encoding methods was used to encode the encoded video data, and said step of processing said at least part of said second signal is dependent on the format of the video data received.

50. (Previously presented) A Digital Versatile Disc device comprising a circuit as claimed in claim 1.

51. (Previously presented) An MPEG decoder comprising a circuit as claimed in claim 1.

52. (Previously presented) A Digital Video Broadcasting device comprising a circuit as claimed in claim 1.

53. (Previously presented) A circuit as claimed in claim 5, wherein said first video data processor is arranged to combine said spatial domain transformed first part of said first signal with said second part of said first signal.

54. (Previously presented) A method as claimed in claim 35, wherein said step of processing said first signal further comprises the step of combining said spatial domain transformed first part of said first signal with said second part of said first signal.

55. (New) The video decoding method as claimed in claim 31, wherein said coding standard information defines variations in the type of data.